User's Manual

SuperRam(tm)

24K MEMORY MASTER(tm)

MORROW DESIGNS

5221 CENTRAL AVENUE
RICHMOND, CA 94804
(415) 524-2101

User's Manual

24K MEMORY MASTER (tm)

INTRODUCTION

The Thinker Toys 24K Memory Master (tm) is our second entry into the field of bank select S-100 memory products. Using the popular 5257 4K x 1 static RAM memory chip with an access time which allows us to guarantee operation with 4MHz Z-80 systems and 5MHz 8085 systems, the 24K Memory Master is compatable with most popular S-100 bank select software. This versatile board can be switched to become selected or deselected in response to any bit of any I/O port; to come up active or inactive on power-up; and to honor or ignore the PHANTOM bus signal. Once selected, the unit is configured as three independently addressable and write protectable 8K blocks, with addressing allowed at the beginning of any 8K boundary.

Of course, the 24K Memory Master also offers the reliability and economy that come with all Morrow Designs (tm), as well as service that is unmatched in the industry-- it's another Thinker Toys product you can bank on.

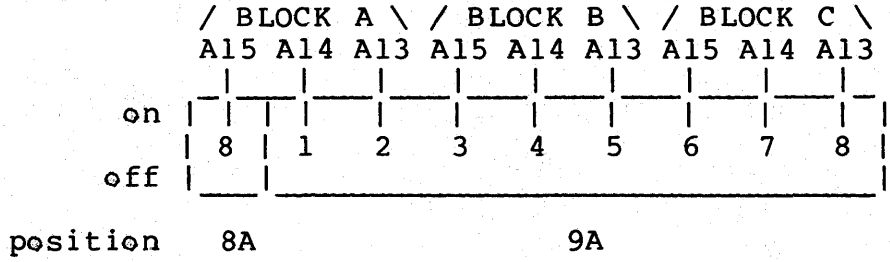
IMPORTANT NOTE: TO AVOID ELECTRICAL DAMAGE TO YOUR MEMORY MASTER BOARD, TURN OFF THE POWER IN YOUR COMPUTER BEFORE INSTALLING OR REMOVING THE BOARD.

MEMORY ADDRESSING

The 24K Memory Master is configured as three blocks of 8K bytes each. Each block can be addressed on an 8K boundary. Thus a block may begin at 0000H, 2000H, 4000H, and so forth up to the last 8K boundary - E000H. The addressing need not be consecutive and may even overlap.

DIP switch 9A (at the top right hand side of the board) and paddle #8 of DIP switch 8A are the address selection switches. Each of these 9 paddles either grounds (when set to "on") or pulls high (when set to "off") one input of a 74LS266 Exclusive Nor gate. The other input is one of the three address lines A13 to A15, buffered and inverted by 74LS04's. Sets of three of these 74LS266 equality gates will select their respective 8K memory block if and only if the S-100 address lines A13 to A15 exactly correspond to the setting of the appropriate paddles of the DIP switches. Thus if the last three paddles of DIP switch 9A are all set to off, or high, then the inverted address lines 13 to 15 must also be high (meaning that the actual address lines are low) in order to select block "C". In this case, selection will only occur when memory between 0000H and 1FFFH is being selected.

The diagram below depicts memory selection switches 8A and 9A and shows the correspondence between the paddles and the three 8K blocks of memory which they govern.

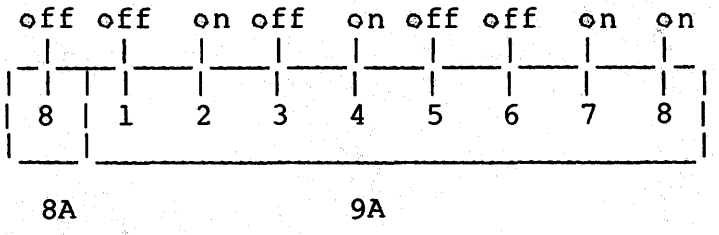


MEMORY ADDRESSING TABLE

The following table shows the relationship between switch settings of the three addressing paddles controlling an 8K memory block and the starting address of that 8K block. The table applies equally to blocks A, B, or C.

Starting Address		A15	A14	A13	Corresponding	
Hex	Octal				hex digit	binary digit
0000	000:000	off	off	off	0	0000
2000	040:000	off	off	on	2	0010
4000	100:000	off	on	off	4	0100
6000	140:000	off	on	on	6	0110
8000	200:000	on	off	off	8	1000
A000	240:000	on	off	on	A	1010
C000	300:000	on	on	off	C	1100
E000	340:000	on	on	on	E	1110

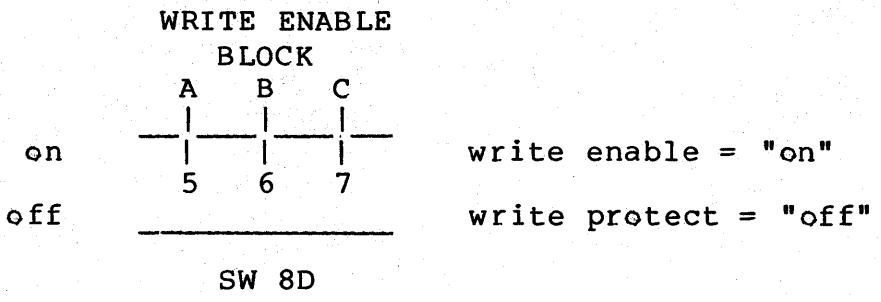
As an example of addressing the 24K Memory Master board, the following switch positions will set the unit to the 24K of memory starting at the second 8K boundary of memory - 2000H.



In this example, Block A occupies memory between 2000H and 3FFFH, Block B occupies memory between 4000H and 5FFFH, and Block C occupies memory between 6000H and 7FFFH.

WRITE PROTECTION

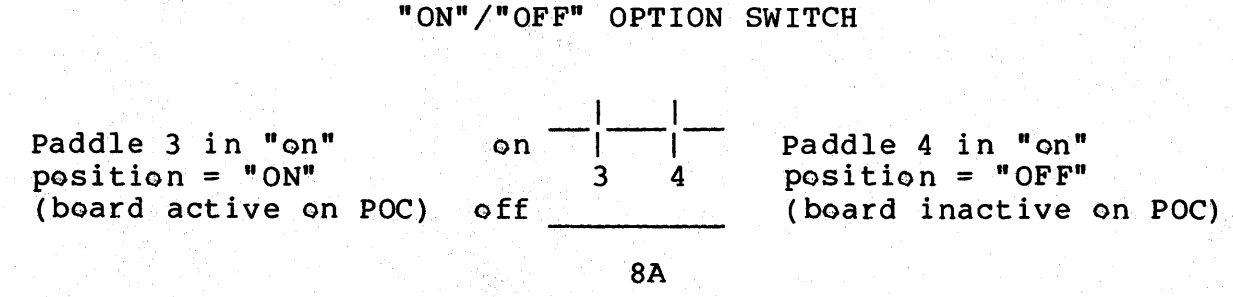
The fifth, sixth, and seventh paddles of DIP switch 8A are the Write Enable switches controlling the three blocks of memory on the 24K Memory Master board. The CPU can write into an 8K block of memory when the paddle associated with that block is in the "on" position. If the paddle is in the "off" position, the entire block is protected and cannot be altered. The association between paddle position and memory block is shown in the figure below.



COMING UP ENABLED OR DISABLED ON POWER-ON-CLEAR

Paddles three and four of DIP switch 8A control whether the Memory Master will come up active or inative on Power-On-Clear. Paddle 3 is the "ON" switch and paddle 4 is the "OFF" switch. In this case "ON" means that the board will be active on Power-On-Clear (hereafter called simply POC); "OFF" means the board will come up inactive on POC. For the "ON" option, set paddle 3 to the "on" position and paddle 4 to the "off" position. For the "OFF" option, set paddle 3 to the "off" position and paddle 4 to the "on" position. In no case should paddles 3 and 4 of the DIP switch at position 8A be set to the same position.

The figure below depicts the "ON" and "OFF" switches of DIP switch 8A.



PADDLE 3 MUST NOT BE IN THE SAME POSITION AS PADDLE 4

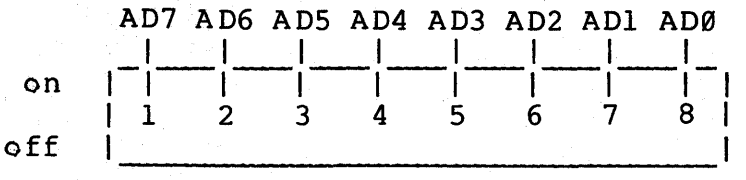
BOARD SELECTION BY I/O ADDRESS -- BANK SELECTION

The purpose of "Bank Selection" is to allow more memory in a system than the CPU can normally address. This is accomplished by assigning a board not only a memory address somewhere within the 64K range of addressable memory, but also an I/O port number between Ø and 255. Thus two boards can share the same memory address, yet have a different I/O address. If a system software scheme takes care to disable one board (by outputting an appropriate byte to the board's I/O port number) before enabling another board (again by outputting the proper byte to its port number), many memory boards can occupy the same memory space without causing any conflict.

With the 24K Memory Master, two assignments must be made for each board in order to operate under a bank select scheme. First an I/O port number must be decided upon; and second, a data bit within that port must be chosen to act as a switch to enable the board or disable it when a byte is written to the I/O port which is assigned to the board. If, for example, a board is assigned I/O port number 4ØH, and further assigned data bit Ø within that port, then the board will be activated when bit Ø of the CPU's A register is on and an "OUT 4ØH" instruction is issued by the CPU. Conversely, the same board will be disabled when the CPU executes an "OUT 4ØH" instruction and bit Ø of the A register is off. (The A register is the CPU's accumulater). In either case the board will remain selected or deselected until the CPU executes an "OUT 4ØH" instruction again and changes the board's selection state or a Power-On-Clear takes place. POC will select or deselect the board according to the setting of paddles 3 and 4 of DIP switch 8A, as described above.

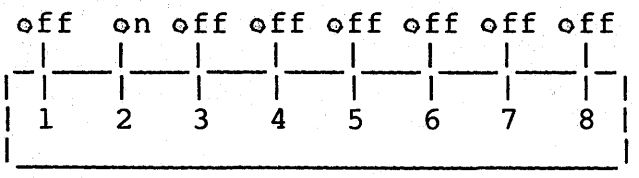
DIP switch 7A, the leftmost switch on the 24K Memory Master board, controls the selection of the I/O port number to which the board is assigned. Paddles 1 through 8 on this switch may be thought of as representing the 8 address bits of the I/O port, with paddle 1 representing bit 7, paddle 2 representing bit 6, and so on through paddle 8 representing bit Ø. This assignment scheme is illustrated in the figure below.

I/O PORT ADDRESSING -- DIP SWITCH 7A



A paddle in the "off" position is to be taken as a cleared bit, while a paddle in the "on" position sets the bit. Thus, if all the paddles of the switch are turned to the "off" position, Ø would be the I/O port number assigned to the Memory Master board. When all the paddles of DIP switch 7A are in the "on" position, 255 (FF Hex or 377 Octal) is the I/O port number which is used to

select or deselect the board. To set the board to, say, device 40H, the following settings should be used.



7A

BOARD SELECTION BY DATA BIT -- BANK SELECTION

Once the I/O port number of the Memory Master board has been determined, there remains the selection of the data bit which will activate or deactivate the board during "OUT" instructions to the selected port.

There is a 16 pin jumber block consisting of two columns of 8 pins each located between columns 6 and 7 of the Memory Master circuit board. Vertically it straddles rows B, C, and D. This jumper block is used to assign a data bit to the bank selection logic on the board. The silk screened legend on the circuit board names the top pair of pins "DATA0" and the bottom pair "7". By jumpering one of the horizontal pairs of pins with the slide-on jumper included with the Memory Master board, the user can select the corresponding bit to activate or deactivate the board. The 16 pin jumper block is shown below with all pairs numbered.

DATA BIT JUMPER SELECTION

	DATA0	* *	jumper a horizontal pair to
16 pin jumper	DATA1	* *	select activation data bit
block located	DATA2	* *	
between columns	DATA3	* *	no pair jumpered and switch
6 and 7 and	DATA4	* *	8A paddle 3 on and paddle 4
straddling rows	DATA5	* *	off will cause the board to
B, C, and D	DATA6	* *	always be activated
	DATA7	* *	

As an example, with the highest pair of pins jumpered, and the board addressed as I/O port 40H, and "OUT 40H" instruction with data bit 0 set in the accumulator will activate the board, while any "OUT 40H" instruction with data bit 0 cleared will de-activate the board. In other words, an "OUT 40H" executing with, say, a 71H in the accumulator will select while an "OUT 40H" with a 72H will deselect.

The fact that any bit can be used as the board select or de-select criteria means that it is possible to assign up to 8 banks of memory using the same I/O port number. Thus, it is possible in a single instruction to turn one bank of memory off and at the

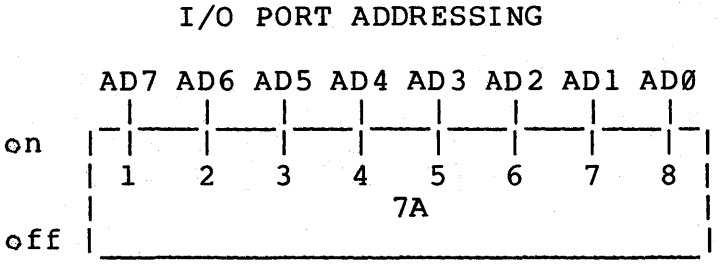
same time turn another on. Being able to select a bit within a port also means that it is possible to have as many as 2048 banks of memory within a single S-100 system - over a 100 MILLION bytes of memory! This should be sufficient for most applications.

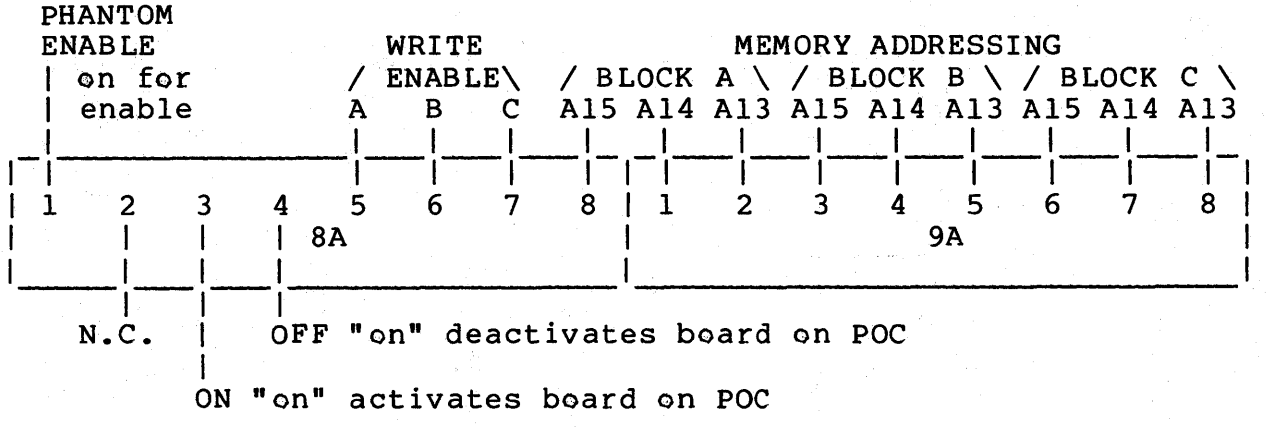
Note that, as indicated in the figure above, the 24K Memory Master can be used as a conventional 24K memory board which pays no attention to any I/O commands. Simply do NOT jumper any pair of pins on the jumper block, set paddle 3 of DIP switch 8A to the "on" position and set paddle 4 of the same switch to the "off" position. This will cause the board to come up selected when power is applied. It will also prevent any bit from deselecting the board, regardless of the I/O port addressing.

PHANTOM ENABLE

Paddle 1 of DIP switch 8A is the Phantom Enable switch. If this paddle is in the "on" position, the Memory Master board will deactivate itself when PHANTOM, line 67 of the S-100 bus, is low (asserted). When paddle 1 is on the "off" position, the Memory Master will not respond to the PHANTOM signal on the bus.

SUMMARY OF SWITCH SETTINGS AND FUNCTIONS





24K MEMORY MASTER PARTS LIST

[ ]	1	5" x 1Ø" printed circuit board w/silk screen legend	
[ ]	4	33Ø Ohm 1/4 watt resistors	
[ ]	3	3.3 k Ohm SIP resistor packs	
[ ]	18	Disk by-pass capacitors -- may vary in value from .Ø1 to .1 microfarads depending on current supplies	
[ ]	4	1.8 microfarad tantalum capacitors	
[ ]	4	39 microfarad tantalum capacitors	
[ ]	3	8 position DIP switches	
[ ]	4	Heat sinks	
[ ]	4	6-32 machine nuts & screws	
[ ]	1	16 pin jumper block	
[ ]	1	Slide-on jumper	
[ ]	13	14-pin low profile sockets	
[ ]	5	16-pin low profile sockets	
[ ]	48	18-pin low profile sockets	
[ ]	4	78Ø5 positive 5 volt regulators	
[ ]	1	74LSØØ quad 2-input NAND gate	9K
[ ]	1	74LSØ2 quad 2-input NOR gate	7F
[ ]	4	74LSØ4 hex inverter	4K,5K,6K,9F
[ ]	1	74LS32 quad 2-input OR gate	7K
[ ]	1	74LS74 dual d-type flip-flop	9H
[ ]	1	74LS138 1 of 8 decoder	8F
[ ]	5	74LS266 quad Exclusive Nor gate	7B,8B,9B,7D,9D
[ ]	1	74S288/S188/6331/82S123 8 x 32 PROM	8D
[ ]	3	74LS367 hex Tri-state buffer	7H,8H,8K
[ ]	48	5257 4K x 1 NMOS Static RAM	1B through 6J

WARNING! IMPROPER ASSEMBLY OF THIS KIT WILL VOID THE WARRANTY. READ THESE INSTRUCTIONS CAREFULLY BEFORE ATTEMPTING TO CONSTRUCT THIS KIT

INVENTORY

Make sure that all the parts listed in the PARTS LIST have been included. Notify Thinker Toys immediately if any parts are missing. Also, quickly return all extra parts.

USE SOCKETS

Sockets are provided for every IC on the 24K Memory Master.

NO REPAIR WORK WILL BE PERFORMED ON ANY RETURNED BOARD WITH ANY IC SOLDERED DIRECTLY TO THE CIRCUIT BOARD

ORIENTATION

When this manual refers to the bottom of the circuit board, it means the edge with the gold S-100 edge connectors. Right and left assume a view from the component side of the board which has the silk screened parts legend embossed over the solder mask.

All IC sockets have their pins numbered, have a 45 degree angle across the corner of pin one, or have a notch at the end which indicates pin one. On the 24K Memory Master, all sockets and all ICs have pin 1 closest to the bottom left corner of the circuit board.

The 1.8 and 39 microfarad tantalum capacitors are polarized. The 1.8 microfarad capacitor's positive end is identified by a circular "tit" where the lead enters the body of the housing. A red band identifies the positive end of the 39 microfarad device. The legend on the circuit board identifies the positive lead of these axial parts with a "+" sign. The by-pass capacitors, which are identified on the legend by an asterisk "*" enclosed by an oval, are not polarized.

The three DIP switch arrays are to be positioned so that the letters and numbers stamped on them are right side up -- that is, paddle 1 should be to the left and paddle 8 on the right.

The SIP resistor packs, historically prone to being inserted backwards, should have their orienting dot nearest the white dot on the legend of the board. On the 24K Memory Master board, this turns out to be to the left for all three SIP packs.

EXAMINE THE BOARD

Visually examine the circuit board for any trace opens or shorts. A concentrated five minute scrutiny will uncover most trace defects. Several hours of scattered, unconcentrated work generally won't reveal anything. Take special care that no short or opens exist on those areas of the circuit board that will be covered by IC sockets. Ohm out any suspicious looking traces for either shorts or discontinuity as appropriate. Return at once any bare board found to be flawed. Such boards will be replaced under warranty.

SOLDERING AND SOLDER IRONS

The most desirable soldering tool for a complex electronic kit is a constant temperature iron with an element regulated at 65Ø degrees F. The tip should be fine so that it can be brought into close contact with the pads of the circuit board. This type of soldering iron is available from Weller or Unger (to name just two) and should be a part of any electronics shop.

There are three important soldering rules that should be followed when building this kit:

1. Do not use an iron that is too cold (less than 6ØØ degrees F.) or too hot (more that 75Ø degrees F.).

2. Do not hold the iron against a pad for more than about six seconds at a time.

3. Do not apply excessive amounts of solder.

The recommended procedure for soldering components to the circuit board is as follows:

1. Bring the iron in contact with BOTH the component lead AND the pad.

2. Apply a SMALL amount of solder at the point where the iron, component lead, and the pad ALL make contact.

3. After the initial application of solder and when it has flowed to the pad and component lead, the heat of the iron will have transferred to BOTH the pad AND the lead. Apply a small amount of additional solder to cover the joint between the pad and the lead. DO NOT PILE SOLDER ON THE JOINT! EXCESSIVE HEAT AND SOLDER CAUSE PADS AND LEADS TO LIFT FROM THE CIRCUIT BOARD. ALSO, EXCESSIVE SOLDER IS THE PRIMARY CAUSE FOR BOARD SHORTS AND BRIDGED CONNECTIONS.

PROTECT YOUR EYES WHEN YOU CLIP COMPONENT LEADS AFTER SOLDERING

[ ] Install and solder the 4 330 Ohm 1/4 watt resistors. Clip the excess leads from the parts.

[ ] Install and solder the 18 pin sockets first, then the 16 and 14 pin sockets in that order. By installing the sockets in this order, a smaller sized socket will never be placed in a larger sized position.

[ ] Install and solder the three SIP resistor packs. Be careful that the orienting dots are pointing to the left.

[ ] Install and solder the 4 axial lead 1.8 microfarad tantalum capacitors. The circular "tit" identifying the positive end is to face toward the bottom of the circuit board when the part is installed. Clip the excess leads from the parts.

[ ] Install and solder the 4 axial lead 39 microfarad tantalum capacitors. The red band identifying the positive end is to face toward the bottom of the circuit board when the part is installed. Clip the excess leads from the parts.

[ ] Install and solder the three DIP switch arrays. Switch 1 is to be positioned to the left when the part is installed.

[ ] Install, solder, and clip the leads of the eighteen by-pass capacitors whose positions are identified by an oval with an asterisk "*" in the middle.

[ ] Install and solder the 16 pin jumper block just to the right of the RAM array. Its position is marked by a rectangular outline with "DATA0" at the top and "DATA7" at the bottom. Make sure that the shorter pins pass through the board.

[ ] Bend the leads of the four 7805 regulators and insert them in the circuit board. Place a heat sink between the 7805 and the board. Work a screw from the back of the board through the board, heat sink, and regulator in that order and hand tighten onto a nut at the top of the regulator. Solder the leads and adjust the heat sinks so that they are square with the board. Finally, tighten the nut and screw.

CLEAN AND EXAMINE THE BOARD

Use flux cleaner to remove solder rosin residue. Examine the circuit board carefully for shorts, solder bridges, or pins on sockets that have not been soldered.

HOW TO FIND WHERE TO PLACE PARTS

For parts placement, please see the silk screened legend on the printed circuit board. ICs may vary from those marked on the legend if they are listed as alternate ICs (following a slash) in the Parts List.

DO NOT INSERT ANY INTEGRATED CIRCUITS AT THIS TIME

Before inserting any IC in its socket, the following check-out procedure must be performed:

1. Re-check the back of the circuit board for solder shorts and bridged connections and for pins of IC sockets that have not been soldered. These unsoldered pins can cause problems which are often intermittant and usually hard to find.

2. Re-check components for orientation. Also make sure all components to be soldered have been soldered.

3. With an Ohm Meter, check for shorts between the +5 Volt lead of the 7805 regulators and ground. The output pins of the regulators are on the right side of the part. Check for shorts between S-100 pin 1 or 51 (+8V) and ground. On the S-100 bus, ground is on pins 50 and 100.

4. Place the board WITHOUT ICs into a bus slot of an otherwise empty system and power up the system. In case of smoke power down immediately and investigate.

5. With a VOM or scope, check the regulators for +5V. Next, check for +5V and ground on all IC sockets. If everything is OK, power down and proceed to IC insertion.

IC INSERTION

If an IC insertion tool is not available, IC leads should be straightened a ROW at a time, not by the individual PIN. An edge of a stright sided table is an excellent device for this purpose. Hold the IC by the plastic case, place one row of legs against a flat surface and push very slightly. Repeat with the opposite row. Continue this procedure until the legs of the IC can be put into its socket with a minimum of effort.

When the IC is inserted into its socket, take care that one or more pins are NOT BENT UNDERNEATH ITS PLASTIC PACK. This is a very common occurance and can escape even a fairly careful visual inspection. BENT IC PINS ARE THE MOST COMMON BOARD FAULT IN KITS THAT ARE BUILT IN THE FIELD!

If IC pins are bent under the pack during insertion, use a pair of long nose pliers to straighten them and try again. When an IC must be removed from its socket, use an IC remover, a test clip (another must for any electronics shop), or a small enough screw driver so that its blade can fit between the plastic case of the IC and the socket. DO NOT ATTEMPT TO REMOVE AN IC WITH YOUR FINGERS. Very often the pins will bend and cut a finger as the IC pops out of its socket.

Once the ICs have been inserted, check once again for bent pins. Then check twice that all the ICs have been inserted into their sockets with the proper orientation - pin 1 must be pointed toward the lower left of the circuit board. Upside down ICs are usually destroyed upon power up.

IF FOR ANY REASON IT BECOMES NECESSARY TO REMOVE A PART THAT HAS BEEN SOLDERED TO THE CIRCUIT BOARD, CLIP ALL THE LEADS OF THE PART BEFORE REMOVING. THIS WILL REDUCE THE CHANCE OF LIFTING PADS.

POWER UP

If all previous checks have been performed, you are ready to put power to your fully populated board. In an empty system with power off, insert the Memory Master and power up. If the board smokes, power down immediately and investigate. If not, measure the regulated voltages once again.

If any of the voltages have been lost since powering up the bare board, power down and check for upside down ICs. Isolate the possible faulty chip or chips by powering down, removing a section of ICs and powering up again. Continue this sequence until the faulty IC or ICs are found.

BE SURE NEVER TO INSERT OR REMOVE A BOARD WITH POWER ON! THIS MAY DAMAGE THE BOARD

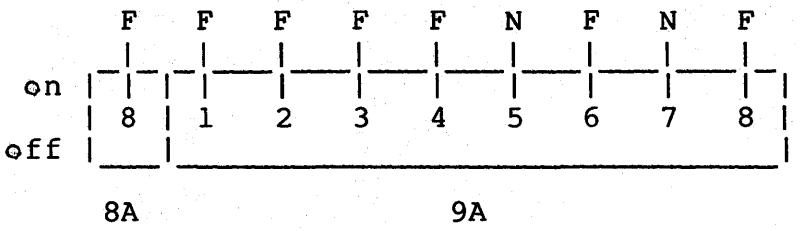
This completes the initial check-out of your Memory Master.

STATIC TEST

Set up

In order to check-out the operation of the 24K Memory Master board, first configure it to function as a simple 24K memory that is addressed as the first 24K of RAM, that is, from ØØØØH at the bottem to 5FFFH at the top. This can be accomplished by making the following switch settings:

1. Set Memory Addressing switches as below --



where "F" = off and "N" = on. This represents ØØØØH - 5FFFH.

2. Set the board to ON (to appear active on POC). As discussed above, this is done by turning paddle 3 of DIP switch 8A "on" and turning paddle 4 of DIP switch 8A "off"

3. Set the board to enable write operations by placing paddles 5 and 6 and 7 of DIP switch 8A to their "on" positions.

4. Set the board to ignore PHANTOM by turning paddle 1 of switch 8A to the "off" position.

5. Set the board to I/O port 4ØH (1ØØQ) by setting paddle 2 of DIP switch 7A to "on" and the rest of the paddles of DIP switch 7A to "off"

6. Do not place the slid-on jumper anywhere on the 16 pin jumper block.

TEST 1: Memory Addressing and Write Protection

With the switch paddles set as indicated above and with the power off, place the Memory Master in a system that has no memory occupying the first 24K. Power the system up.

With a front panel (one that MUST generate the S-1ØØ status signal SWO during memory deposits) or a monitor, examine location ØØØØH, write ØØH in this location, and re-examine it to be sure that it now contains a ØØ. Now deposit FFH (377Q) in this same location and read it back. Now set paddle 5 of DIP switch 8A to "off", and attempt to change the FF in location ØØØØH to another number -- you should not be able to alter this location now. Set

paddle 5 of 8A back to "on". Verify that location ØØØØH can once again be altered. Repeat the above procedure first at location 2ØØØH using paddle 6 of 8A and then again at location 4ØØØH with paddle 7 of 8A.

TEST 2: Bank Selection

Place the slide-on jumper across the two pins labled DATAØ on the 16 pin jumper block. With a Ø in the CPU's accumulator, execute an "OUT 4ØH" command. You should now have lost access to the Memory Master board. Now execute an "OUT 4ØH" command with a 1 in the CPU's accumulator. The Memory Master should now be once again accessable.

TEST 3: POC - ON/OFF

With a jumper still across DATAØ of the 16 pin jumper block, make sure that you can still access the board. Now turn off the power and back on again and again verify that the board can be accessed. Next, on DIP switch 8A, turn paddle 3 "off" and turn paddle 4 "on". Power down and power back up again. The Memory Master should be disabled. Execute an "OUT 4ØH" instruction with a 1 in the CPU's accumulator. This should reactivate the Memory Master.

This completes the static system tests. The following pages contain a full fleged memory diagnostic.

MEMORY DIAGNOSTIC

The memory test described below was designed by Phil Meads of William Brobeck Associates to exercise the most sensitive circuitry of the memory chips -- the address buffers. The test starts from the middle and works its way outward alternately to the top and bottom of memory. This type of test inverts the address lines more often than sequential ones. This continual inversion process punishes and eventually breaks down weak or faulty address buffers in the device.

USING THE TEST

The test itself must be placed in an area which is different than the location of the board(s) to be tested. The test starts on a page boundary to make the task of relocating the binary code easier.

There are two parameters in the test to be set by the user:

(1) The number of 4K blocks to be tested -- keep in mind that there are four 4K blocks per board. This constant is called BLKCNT and is located at the eleventh byte of the test.

(2) The starting page number of the lowest 4K block to be tested is called PAGENO and is located at the ninth byte of the test.

When testing more than one 4K block of memory, be sure that they occupy contiguous memory.

The page number of the position of the test itself must be entered wherever a $(YYY)_8$ or $(YY)_{16}$ occurs in the test listing. This is necessary because JMP and CALL need both the page number and the location within the page to execute correctly.

The only other thing to remember when loading the test is that it must be placed at the starting address of a page.

Start the test at the first instruction. Once started, the test will run continuously unless an error is detected. If the test encounters an error, all the data pertinent to this error is stored in the last ten locations of the test. After storing this data, the test comes to a dynamic halt at the label STALL. The test may be restarted by stopping the computer and restarting it at the POP PSW instruction following JMP STALL. The user may also restart the test from the beginning. If errors indicate the board is malfunctioning, return it as soon as possible for service.

MEMORY TEST PROGRAM FOR 4K NMOS RAMS

Octal

```
YYY  000 061 175 YYY     START  LXI   SP,STACK    INITIALIZE STACK POINTER
     003 001 000 000            LXI   B,0         INITIALIZE CYCLE COUNT
     006 305            NEWCYL  PUSH  B           UPDATE CYCLE COUNT
     007 006 100                MVI   B,PAGENO    STARTING ADDR OF TEST MEM
     011 016 004                MVI   C,BLKCNT    # OF 4K BLOCKS TO TEST
     013 041 377 007    LOOP    LXI   H,7:377Q    HALF SIZE OF MEMORY -1
     016 170                    MOV   A,B
     017 204                    ADD   H           CALCULATE MIDDLE
     020 147                    MOV   H,A           OF CURRENT BLOCK
     021 345                    PUSH  H           SAVE INITIAL ADDRESS
     022 315 114 YYY    WRITE   CALL  TWORD       GET TEST WORD
     025 167                    MOV   M,A         STORE
     026 315 123 YYY            CALL  COMP        COMPLEMENT ADDRESS
     031 315 114 YYY            CALL  TWORD       GET TEST WORD
     034 167                    MOV   M,A         STORE
     035 315 134 YYY            CALL  INCR        COMPLEMENT & DECREMENT
     040 302 022 YYY            JNZ   WRITE         ADDRESS
     043 341                    POP   H           RECOVER INITIAL ADDRESS

YYY  044 315 114 YYY     READ    CALL  TWORD       GET TEST WORD
     047 256                    XRA   M           COMPARE
     050 304 145 YYY            CNZ   ERROR
     053 315 123 YYY            CALL  COMP        COMPLEMENT ADDRESS
     056 315 114 YYY            CALL  TWORD       GET TEST WORD
     061 256                    XRA   M           COMPARE
     062 304 145 YYY            CNZ   ERROR
     065 315 134 YYY            CALL  INCR        COMPLEMENT & DECREMENT
     070 302 044 YYY            JNZ   READ          ADDRESS

YYY  073 076 020                MVI   A,20Q      ADVANCE
     075 200                    ADD   B             THE
     076 107                    MOV   B,A           BLOCK
     077 015                    DCR   C           DECREMENT BLOCK COUNT
     100 302 013 YYY            JNZ   LOOP
     103 173                    MOV   A,E         CALCULATE NEW
     104 306 207                ADI   135           BASE FOR
     106 137                    MOV   E,A           TEST WORD
     107 301                    POP   B
     110 003                    INX   B           INCREMENT CYCLE COUNT
     111 303 006 YYY            JMP   NEWCYL

     114 175            TWORD   MOV   A,L         GET LOWER BYTE OF ADDRESS
     115 007                    RLC               ROTATE
     116 207                    ADD   A           SHIFT
     117 204                    ADD   H           ADD HIGHER BYTE OF ADDR
     120 203                    ADD   E           ADD BASE
     121 127                    MOV   D,A         SAVE TEST WORD
     122 311                    RET
```

```
YYY  123 174           COMP   MOV   A,H      COMPLEMENT THE UPPER
     124 356 017              XRI   17Q        BYTE ADDRESS
     126 147                  MOV   H,A        WITH RESPECT TO MEM SIZE
     127 175                  MOV   A,L      COMPLEMENT THE LOWER
     130 356 377              XRI   377Q       BYTE OF THE
     132 157                  MOV   L,A        ADDRESS
     133 311                  RET

YYY  134 315 123 YYY  INCR   CALL  COMP     RESTORE ADDR TO NORMAL SIZE
     137 053                  DCX   H        DECREMENT
     140 300                  RNZ             TEST IF LOWER BYTE ZERO
     141 170                  MOV   A,B      TEST UPPER BYTE EQUAL
     142 075                  DCR   A          TO BLOCK
     143 274                  CMP   H          BOUNDARY
     144 311                  RET

YYY  145 345           ERROR  PUSH  H        SAVE ERROR ADDRESS
     146 305                  PUSH  B        SAVE CURRENT BLOCK
     147 325                  PUSH  D        SAVE TEST WORD
     150 365                  PUSH  PSW      SAVE ERROR BITS
     151 303 151 YYY  STALL  JMP   STALL    DYNAMIC HALT
     154 361                  POP   PSW      RESTORE
     155 321                  POP   D          THE
     156 301                  POP   B          STATE OF
     157 341                  POP   H          THE CPU
     160 311                  RET

YYY  161 000           TABLE  DB    0        FLAGS
     162 000                  DB    0        ACC - ONES ARE ERROR BITS
     163 000                  DB    0        E - CURRENT RANDOM OFFSET
     164 000                  DB    0        D - CURRENT TEST WORD
     165 000                  DB    0        C - CURRENT BLOCK COUNT
     166 000                  DB    0        B - CURRENT BLOCK PAGE
     167 000 000              DW    0        HL - ERROR ADDRESS
     171 000 000              DW    0        RETURN ADDRESS
     173 000 000              DW    0        CYCLE COUNT
     175 000 000       STACK  DW    0
```

MEMORY TEST PROGRAM FOR 4K NMOS RAMS

Hex

```
YY  00    31 7D YY      START  LXI   SP,STACK
    03    01 00 00             LXI   B,0
    06    C5           NEWCYL  PUSH  B
    07    06 40                MVI   B,PAGENO
    09    0E 04                MVI   C,BLKCNT
    0B    21 FF 07     LOOP    LXI   H,7:377Q
    0E    78                   MOV   A,B
    0F    84                   ADD   H
    10    67                   MOV   H,A
    11    E5                   PUSH  H
    12    CD 4C YY     WRITE   CALL  TWORD
    15    77                   MOV   M,A
    16    CD 53 YY             CALL  COMP
    19    CD 4C YY             CALL  TWORD
    1C    77                   MOV   M,A
    1D    CD 5C YY             CALL  INCR
    20    C2 12 YY             JNZ   WRITE
    23    E1                   POP   H

YY  24    CD 4C YY     READ    CALL  TWORD
    27    AE                   XRA   M
    28    C4 65 YY             CNZ   ERROR
    2B    CD 53 YY             CALL  COMP
    2E    CD 4C YY             CALL  TWORD
    31    AE                   XRA   M
    32    C4 65 YY             CNZ   ERROR
    35    CD 5C YY             CALL  INCR
    38    C2 24 YY             JNZ   READ

YY  3B    3E 10                MVI   A,20Q
    3D    80                   ADD   B
    3E    47                   MOV   B,A
    3F    0D                   DCR   C
    40    C2 0B YY             JNZ   LOOP
    43    7B                   MOV   A,E
    44    C6 87                ADI   135
    46    5F                   MOV   E,A
    47    C1                   POP   B
    48    03                   INX   B
    49    C3 06 YY             JMP   NEWCYL

YY  4C    7D           TWORD   MOV   A,L
    4D    07                   RLC
    4E    87                   ADD   A
    4F    84                   ADD   H
    50    83                   ADD   E
    51    57                   MOV   D,A
    52    C9                   RET
```

```
YY  53    7C          COMP   MOV    A,H
    54    EE OF              XRI    17Q
    56    67                 MOV    H,A
    57    7D                 MOV    A,L
    58    EE FF              XRI    377Q
    5A    6F                 MOV    L,A
    5B    C9                 RET

YY  5C    CD 53 YY    INCR   CALL   COMP
    5F    2B                 DCX    H
    60    C0                 RNZ
    61    78                 MOV    A,B
    62    3D                 DCR    A
    63    BC                 CMP    H
    64    C9                 RET

YY  65    E5          ERROR  PUSH   H
    66    C5                 PUSH   B
    67    D5                 PUSH   D
    68    F5                 PUSH   PSW
    69    C3 69 YY    STALL  JMP    STALL
    6C    F1                 POP    PSW
    6D    D1                 POP    D
    6E    C1                 POP    B
    6F    E1                 POP    H
    70    C9                 RET

YY  71    00          TABLE  DB     0       FLAGS
    72    00                 DB     0       ACC - ONES ARE ERROR BITS
    73    00                 DB     0       E - CURRENT RANDOM OFFSET
    74    00                 DB     0       D - CURRENT TEST WORD
    75    00                 DB     0       C - BLOCKS LEFT TO TEST
    76    00                 DB     0       B - CURRENT BLOCK PAGE
    77    00 00              DW     0       HL - ERROR ADDRESS
    79    00 00              DW     0       RETURN ADDRESS
    7B    00 00              DW     0       CYCLE COUNT
    7D    00 00       STACK  DW     0
```